In the Claims:

Please amend Claims 23, 29, 43, and 49 as indicated below. The status of all claims is as follows:

1-22 (Cancelled)

23. (Previously Presented) A thin film transistor matrix device comprising:

an insulating substrate;

a plurality of thin film transistors arranged on the insulating substrate in a matrix;

a plurality of picture element electrodes arranged on the insulating substrate in a matrix and connected to the thin film transistors;

a plurality of bus lines for commonly connecting the gates of the thin film transistors, the bus lines being made of a first conducting film;

a first insulating film formed on the first conducting film;

a second conducting film formed on the first insulating film; and

a second insulating film formed on the first insulating film and the second conducting film;

wherein, outside an image display ~~region,~~ region in which the plurality of picture elements are formed,

a first contact hole is formed in the first insulating film and the second insulating film through the first conducting film,

a second contact hole is formed in the second insulating film through the second conducting film, ~~and~~

~~the first conducting film and the second conducting film electrically connect by~~ a third conducting film ~~which~~ is formed between the first contact hole and the second contact hole on the second insulating ~~film.~~ film,

the first conducting film is connected to the third conducing film via the first contact hole, and

the second conducting film is connected to the third conducting film via the second contact hole.

24. (Previously Presented) A thin film transistor matrix device according to claim 23, wherein

a plurality of gate insulating films of the plurality of thin film transistors are made of the first insulating film.

25. (Previously Presented) A thin film transistor matrix device according to claim 23, wherein

the third conducting film is formed simultaneously with the plurality of picture element electrodes.

26. (Previously Presented) A thin film transistor matrix device according to claim 23, wherein the third conducting film and the plurality of picture elements are made by Indium Tin Oxide.

27. (Previously Presented) A thin film transistor matrix device according to claim 23, wherein

the first contact hole comprises a first hole of the first insulating film and a second hole of the second insulating film, and

an axis of the first hole coincides with an axis of the second hole.

28. (Previously Presented) A thin film transistor matrix device according to claim 23, wherein

the first contact hole comprises a first hole of the first insulating film and a second hole of the second insulating film, and

the first contact hole continues from the first hole to the second hole.

29. (Currently Amended) A thin film transistor matrix device comprising:

an insulating substrate;

a plurality of thin film transistors arranged on the insulating substrate in a matrix;

a plurality of picture element electrodes arranged on the insulating substrate in a matrix and connected to the thin film transistors;

a plurality of bus lines for commonly connecting the gates of the thin film transistors, the bus lines being made of a first conducting film;

a first insulating film formed on the first conducting film;

a first connection line for commonly crossing the plurality of bus lines, the first connection line being made of a second conducting film formed on the first insulating film; and

a second insulating film formed on the first insulating film and the second conducting film,

wherein, outside an image display ~~region,~~ region in which the plurality of picture element electrodes are formed,

a first contact hole is formed in the first insulating film and the second insulating film through the first conducting film,

a second contact hole is formed in the second insulating film through the second conducting film, ~~and~~

~~each of the plurality of bus lines is electrically connected to the first connection line through~~ a third conducting film ~~which~~ is formed between the first contact hole and the second contact hole on the second insulating ~~film.~~ film,

each of the plurality of bus lines is connected to the third conducting film via the first contact hole, and

the first connection line is connected to the third conducting film via the second contact hole.

30. (Previously Presented) A thin film transistor matrix device according to claim 29, wherein

a plurality of gate insulating films of the plurality of thin film transistors are made of the first insulating film.

31. (Previously Presented) A thin film transistor matrix device according to claim 29, wherein

the third conducting film is formed simultaneously with the plurality of picture element electrodes.

32. (Previously Presented) A thin film transistor matrix device according to claim 31, wherein

the third conducting film and the plurality of picture elements are made by Indium Tin Oxide.

33. (Previously Presented) A thin film transistor matrix device according to claim 29, wherein

the first contact hole comprises a first hole of the first insulating film and a second hole of the second insulating film, and

an axis of the first hole coincides with an axis of the second hole.

34. (Previously Presented) A thin film transistor matrix device according to claim 29, wherein

the first contact hole comprises a first hole of the first insulating film and a second hole of the second insulating film, and

the first contact hole continues from the first hole to the second hole.

35. (Previously Presented) A thin film transistor matrix device comprising:

an insulating substrate;

a plurality of thin film transistors arranged on the insulating substrate in a matrix;

a plurality of picture element electrodes arranged on the insulating substrate in a matrix and connected to the thin film transistors;

a plurality of gate bus lines for commonly connecting the gates of the thin film transistors, the gate bus lines being made of a first conducting film;

a first insulating film formed on the first conducting film;

a first connection line for commonly crossing the plurality of gate bus lines, the first connection line being made of a second conducting film formed on the first insulating film;

a plurality of drain bus lines for commonly connecting the drains of the thin film transistors, the drain bus lines being made of the second conducting film;

a second connection line for commonly crossing the plurality of drain bus lines, the second connection line being made of the first conducting film; and

a second insulating film formed on the first insulating film and the second conducting film,

wherein, outside an image display region,

a first contact hole is formed in the first insulating film and the second insulating film through the first conducting film,

a second contact hole is formed in the second insulating film through the second conducting film, and

each of the plurality of gate bus lines is electrically connected, through a third conducting film which is formed between the first contact hole and the second contact hole on the second insulating film, to the second connection line through a resistance.

36. (Previously Presented) A thin film transistor matrix device according to claim 35, wherein

a plurality of gate insulating films of the plurality of thin film transistors are made of the first insulating film.

37. (Previously Presented) A thin film transistor matrix device according to claim 35, wherein

the third conducting film is formed simultaneously with the plurality of picture element electrodes.

38. (Previously Presented) A thin film transistor matrix device according to claim 35, wherein

the third conducting film and the plurality of picture elements are made by Indium Tin Oxide.

39. (Previously Presented) A thin film transistor matrix device comprising:

an insulating substrate;

a plurality of thin film transistors arranged on the insulating substrate in a matrix;

a plurality of picture element electrodes arranged on the insulating substrate in a matrix and connected to the thin film transistors;

a plurality of gate bus lines for commonly connecting the gates of the thin film transistors, the gate bus lines being made of a first conducting film;

a first insulating film formed on the first conducting film;

a first connection line for commonly crossing the plurality of gate bus lines, the first connection line being made of a second conducting film formed on the first insulating film;

a plurality of drain bus lines for commonly connecting the drains of the thin film transistors, the drain bus lines being made of the second conducting film;

a second connection line for commonly crossing the plurality of drain bus lines, the second connection line being made of the first conducting film; and

a second insulating film formed on the first insulating film and the second conducting film,

wherein, outside an image display region,

a first contact hole is formed in the first insulating film and the second insulating film through the first conducting film,

a second contact hole is formed in the second insulating film through the second conducting film, and

each of the plurality of gate bus lines is electrically connected, through a third conducting film which is formed between the first contact hole and the second contact hole on the second insulating film, to each of the plurality of drain bus lines through a resistance.

40. (Previously Presented) A thin film transistor matrix device according to claim 39, wherein

a plurality of gate insulating films of the plurality of thin film transistors are made of the first insulating film.

41. (Previously Presented) A thin film transistor matrix device according to claim 39, wherein

the third conducting film is formed simultaneously with the plurality of picture element electrodes.

42. (Previously Presented) A thin film transistor matrix device according to claim 41, wherein

the third conducting film and the plurality of picture elements are made by Indium Tin Oxide.

43. (Currently Amended) A thin film transistor matrix device comprising:

an insulating substrate;

a plurality of thin film transistors arranged on the insulating substrate in a matrix;

a plurality of picture element electrodes arranged on the insulating substrate in a matrix and connected to the thin film transistors;

a plurality of bus lines for commonly connecting the gates of the thin film transistors, the bus lines being made of a first conducting film;

a first insulating film formed on the first conducting film;

a second conducting film formed on the first insulating film, the second conducting film comprising a non-doped Silicon film, a doped n^+ -type Silicon film, and a metal film; and

a second insulating film formed on the first insulating film and the second conducting film;

wherein, outside an image display ~~region,~~ region in which the plurality of picture element electrodes are formed,

a first contact hole is formed in the first insulating film and the second insulating film through the first conducting film,

a second contact hole is formed in the second insulating film through the second conducting film, ~~and~~

~~the first conducting film and the second conducting film electrically connect by~~ a third conducting film ~~which~~ is formed between the first contact hole and the second contact hole on the second insulating ~~film.~~ film,

each of the plurality of bus lines is connected to the third conducting film via the first contact hole, and

the first connection line is connected to the third conducting film via the second contact hole.

44. (Previously Presented) A thin film transistor matrix device according to claim 43, wherein

a plurality of gate insulating fi1ms of the plurality of thin film transistors are made of the first insulating film.

45. (Previously Presented) A thin film transistor matrix device according to claim 43, wherein

the third conducting film is formed simultaneously with the plurality of picture element electrodes.

46. (Previously Presented) A thin film transistor matrix device according to claim 45, wherein

the third conducting film and the plurality of picture elements are made by Indium Tin Oxide.

47. (Previously Presented) A thin film transistor matrix device according to claim 43, wherein

the first contact hole comprises a first hole of the first insulating film and a second hole of the second insulating film, and

an axis of the first hole coincides with an axis of the second hole.

48. (Previously Presented) A thin film transistor matrix device according to claim 43, wherein

the first contact hole comprises a first hole of the first insulating film and a second hole of the second insulating film, and

the first contact hole continues from the first hole to the second hole.

49. (Currently Amended) A thin film transistor matrix device comprising:

an insulating substrate;

a plurality of thin film transistors arranged on the insulating substrate in a matrix;

a plurality of picture element electrodes arranged on the insulating substrate in a matrix and connected to the thin film transistors;

a plurality of bus lines for commonly connecting the gates of the thin film transistors, the bus lines being made of a first conducting film;

a first insulating film formed on the first conducting film;

a first connection line for commonly crossing the plurality of bus lines, the first connection line being made of a second conducting film formed on the first insulating film, the second conducting film comprising a non-doped Silicon film, a doped n^+ -type Silicon film, and a metal film; and

a second insulating film formed on the first insulating film and the second conducting film,

wherein, outside an image display ~~region,~~ region in which the plurality of picture element electrodes are formed,

a first contact hole is formed in the first insulating film and the second insulating film through the first conducting film,

a second contact hole is formed in the second insulating film through the second conducting film, ~~and~~

~~each of the plurality of bus lines is electrically connected to the first connection line through~~ a third conducting film ~~which~~ is formed between the first contact hole and the second contact hole on the second insulating ~~film.~~ film,

each of the plurality of bus lines is connected to the third conducting film via the first contact hole, and

the first connection line is connected to the third conducting film via the second contact hole.

50. (Previously Presented) A thin film transistor matrix device according to claim 49, wherein

a plurality of gate insulating films of the plurality of thin film transistors are made of the first insulating film.

51. (Previously Presented) A thin film transistor matrix device according to claim 49, wherein

the third conducting film is formed simultaneously with the plurality of picture element electrodes.

52. (Previously Presented) A thin film transistor matrix device according to claim 51, wherein

the third conducting film and the plurality of picture elements are made by Indium Tin Oxide.

53. (Previously Presented) A thin film transistor matrix device according to claim 49, wherein

the first contact hole comprises a first hole of the first insulating film and a second hole of the second insulating film, and

an axis of the first hole coincides with an axis of the second hole.

54. (Previously Presented) A thin film transistor matrix device according to claim 49, wherein

the first contact hole comprises a first hole of the first insulating film and a second hole of the second insulating film, and

the first contact hole continues from the first hole to the second hole.

55. (Previously Presented) A thin film transistor matrix device comprising:

an insulating substrate;

a plurality of thin film transistors arranged on the insulating substrate in a matrix;

a plurality of picture element electrodes arranged on the insulating substrate in a matrix and connected to the thin film transistors;

a plurality of gate bus lines for commonly connecting the gates of the thin film transistors, the gate bus lines being made of a first conducting film;

a first insulating film formed on the first conducting film;

a first connection line for commonly crossing the plurality of gate bus lines, the first connection line being made of a second conducting film formed on the first insulating film;

the second conducting film comprising a non-doped Silicon film, a doped n^+ -type Silicon film, and a metal film;

a plurality of drain bus lines for commonly connecting the drains of the thin film transistors, the drain bus lines being made of the second conducting film;

a second connection line for commonly crossing the plurality of drain bus lines, the second connection line being made of the first conducting film; and

a second insulating film formed on the first insulating film and the second conducting film,

wherein, outside an image display region,

a first contact hole is formed in the first insulating film and the second insulating film through the first conducting film,

a second contact hole is formed in the second insulating film through the second conducting film, and

each of the plurality of gate bus lines is electrically connected, through a third conducting film which is formed between the first contact hole and the second contact hole on the second insulating film, to the second connection line through a resistance.

56. (Previously Presented) A thin film transistor matrix device according to claim 55, wherein

a plurality of gate insulating films of the plurality of thin film transistors are made of the first insulating film.

57. (Previously Presented) A thin film transistor matrix device according to claim 55, wherein

the third conducting film is formed simultaneously with the plurality of picture element electrodes.

58. (Previously Presented) A thin film transistor matrix device according to claim 57, wherein

the third conducting film and the plurality of picture elements are made by Indium Tin Oxide.

59. (Previously Presented) A thin film transistor matrix device comprising:

an insulating substrate;

a plurality of thin film transistors arranged on the insulating substrate in a matrix;

a plurality of picture element electrodes arranged on the insulating substrate in a matrix and connected to the thin film transistors;

a plurality of gate bus lines for commonly connecting the gates of the thin film transistors, the gate bus lines being made of a first conducting film;

a first insulating film formed on the first conducting film;

a first connection line for commonly crossing the plurality of gate bus lines, the first connection line being made of a second conducting film formed on the first insulating film,

the second conducting film comprising a non-doped Silicon film, a doped n^+ -type Silicon film, and a metal film;

a plurality of drain bus lines for commonly connecting the drains of the thin film transistors, the drain bus lines being made of the second conducting film;

a second connection line for commonly crossing the plurality of drain bus lines, the second connection line being made of the first conducting film; and

a second insulating film formed on the first insulating film and the second conducting film,

wherein, outside an image display region,

a first contact hole is formed in the first insulating film and the second insulating film through the first conducting film,

a second contact hole is formed in the second insulating film through the second conducting film, and

each of the plurality of gate bus lines is electrically connected, through a third conducting film which is formed between the first contact hole and the second contact hole on the second insulating film, to each of the plurality of drain bus lines through a resistance.

60. (Previously Presented) A thin film transistor matrix device according to claim 59, wherein

a plurality of gate insulating films of the plurality of thin film transistors are made of the first insulating film.

61. (Previously Presented) A thin film transistor matrix device according to claim 59, wherein

the third conducting film is formed simultaneously with the plurality of picture element electrodes.

62. (Previously Presented) A thin film transistor matrix device according to claim 61, wherein

the third conducting film and the plurality of picture elements are made by Indium Tin Oxide.